Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 70063

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – FEB. 2025

First Semester

VLSI Design

P23VDE03 – FOUNDATIONS OF VLSI CAD

(Regulation 2023)

Time: Three Hours | Maximum: 100 Marks

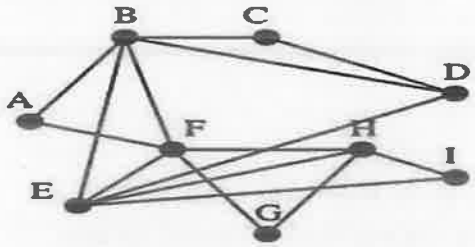
Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

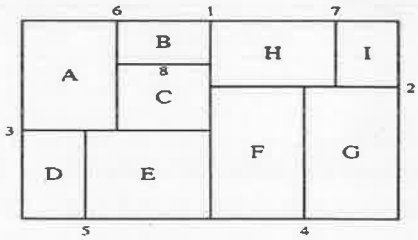
PART – A

(10 x 2 = 20 Marks)

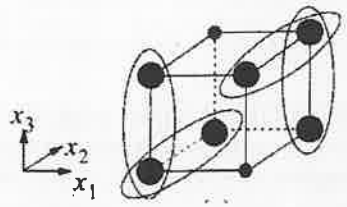
Q.No.	Questions	Marks	KL	CO
1.	Draw the rectangular dual of the graph shown below.	2	K2	CO1



2.	Explain the Kruskal's algorithm with the help of an example.	2	K1	CO1
3.	Write the pseudo code for the simulated annealing algorithm for partitioning.	2	K1	CO2
4.	Consider the pin locations a(2, 6), b(5, 4), c(10, 6), d(7, 2), e(7, 7), f(1, 9), g(3, 5), draw the minimum spanning tree and find the total wire length.	2	K2	CO2
5.	Draw the slicing tree of the floorplan given below.	2	K2	CO3



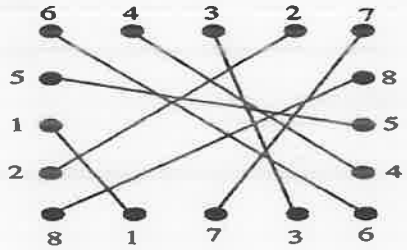
6.	Differentiate Maze running and Line search algorithms for routing.	2	K1	CO3
7.	What is switch level modeling. Illustrate with an example.	2	K1	CO4

8.	 Find the expression corresponding to the prime cover.	2	K3	CO4
9.	Differentiate between ASAP and list scheduling.	2	K1	CO5
10.	Draw a DFG for the code segment given below, **while** $(a > b)$ $a \leftarrow a - b$;	2	K2	CO5

PART – B

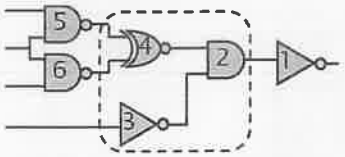
(5 x 13 = 65 Marks)

Q.No.		Questions	Marks	KL	CO
11.	a)	For the switchbox shown in figure below, find maximum independent set, maximum clique, and maximum bipartite subgraph in the permutation graph defined by the matching diagram.	13 (3+3+ 7)	K2	CO1



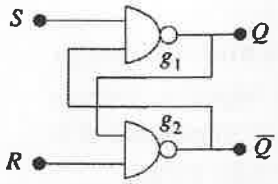
(OR)

	b)	Design an algorithm to delete a given block from a given set of blocks using modified linked list data structure. Once a block is deleted the area occupied by that block becomes vacant tile and the linked list must be updated to take care of this situation.	13	K3	CO1
12.	a)	Apply Kernighan-Lin algorithm and obtain a bipartition for the circuit shown below. Dotted line represents the initial cut.	13	K4	CO2



(OR)

	b)	Consider the circuit in the figure below. Represent it in the cell-port-net data model, the tripartite the graph model, the bipartite graph model and the clique model.	13 (3+3+ 3+4)	K2	CO2



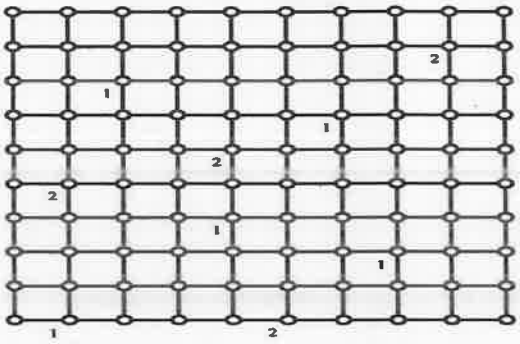
13. a) For the channel TOP = [1, 1, 4, 2, 3, 4, 3, 6, 5, 8, 5, 9] and BOTTOM = [2, 3, 2, 0, 5, 6, 4, 7, 6, 9, 8, 7] draw the horizontal constraint graph (HCG) and the directed vertical constraint graph (VCG). Complete the channel routing using Extended Left Edge Algorithm and Dog Leg Channel routing. Find out the number of tracks required in both the cases. 13 K4 CO3

(OR)

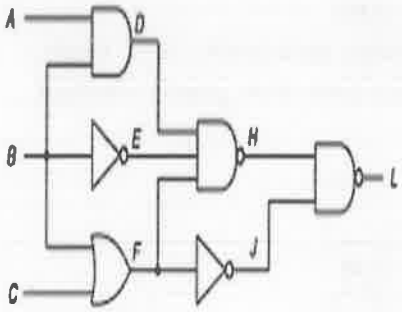
b) For graph in figure, find an RST for each net N1 and N2 such that they do not intersect with each other and 13 K4 CO3

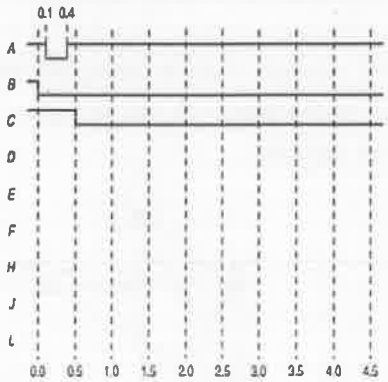
(a) the summation of the cost of these two RST's is minimum,

(b) the maximum of the costs of these two RST's is minimum.



14. a) Apply event-driven simulation technique for the circuit given below using the given waveforms. Show all events and activity lists of each time stamp. Delay of two-input gates -1 ns, delay of three-input gates -1.2 ns, and delay of inverter - 0.6 ns. 13 K3 CO4





(OR)

b) Construct an OBDD for the logic function given in the truth table below using the order (x, y, z) and obtain ROBDD by applying various reduction rules. Clearly draw each step. Check if the complement of h can be obtained from the ROBDD from part b. Prove your answer. 13 K3 CO4

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

15. a) Consider the following operations K2 CO5

$a = i + j;$
$b = k + l;$
$c = a + b;$
$d = b - n;$
$e = c + m;$
$f = c + e;$

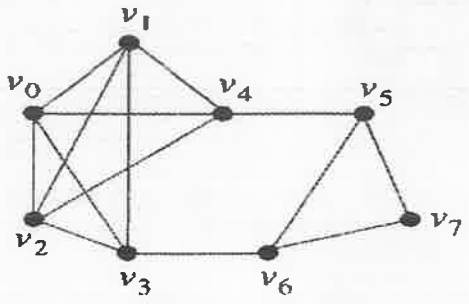
Assume that the resource type is a two input adder/subtractor and its delay is 50ns.

i. Determine a minimum latency schedule assuming only 2 resources are available. Also show the hardware level realization for this scheduling using registers, multipliers, and adders. 8

ii. If cycle time is 100ns, determine a minimum latency schedule with the reduction of resource usage as a secondary goal. 5

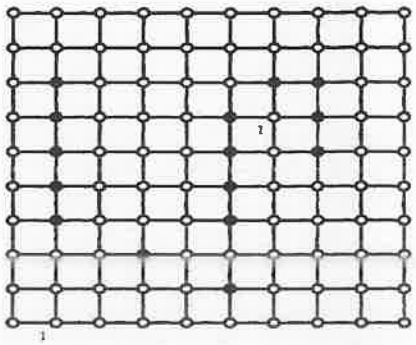
(OR)

b) Write the pseudo code to compute the clique partitioning of a graph. Apply it on the graph shown in figure below and show graphs obtained after each iteration. 13 K2 CO5



PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Given the following 14 rectangles with their dimensions specified, write a program that will arrange all these rectangles within 5000 sq. units of area, if possible, or otherwise minimize the area required. The dimensions (width x height) of the rectangles are $R_1 = 15\ X\ 15, R_2 = 25\ X\ 15, R_3 = 10\ X\ 30, R_4 = 30\ X\ 20,$ $R_5 = 10\ X\ 15, R_6 = 20\ X\ 5, R_7 = 10\ X\ 25,\ R_8 = 30\ X\ 15,$ $R_9 = 10\ X\ 65, R_{10} = 10\ X\ 25, R_{11} = 20\ X\ 20, R_{12} = 10\ X\ 20,$ $R_{13} = 30\ X\ 15, R_{14} = 40\ X15.$	15	K4	CO1
		(OR)			
	b)	 The terminals of a two-terminal net are marked by '1'. The shaded circles indicate blocked vertices. Using the Lee's algorithm, Soukup's algorithm, and Hadlock's algorithm, find the path for N_1 and the number of nodes explored.	15 (8+7)	K5	CO3